What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of synchronizing an output signal with a first clock signal, the method comprising:

receiving said first clock signal;

delaying said received first clock signal to produce a delayed clock signal;

providing a first timing signal associated with one of a rising and falling edge of said delayed clock signal;

providing a second timing signal associated with the other of a rising and falling edge of said delayed clock signal;

adjusting the relative timing of at least one of said first and second timing signals to produce substantially equal time durations between the occurrence of said first and second timing signals; and

using said first and second timing signals to produce said output signal synchronized with said first clock signal, said output signal having a substantially symmetric duty cycle.

2. A method of claim 1 wherein said output signal is a data output signal.

3. A method of claim 1 wherein said output signal is a timing signal.

4. The method of claim 1, further comprising generating said output signal from said first and second timing signals, said output signal being generated by generating a rising edge of the output signal in response to the first timing signal and generating a falling edge of the output signal in response to the second timing signal.

5. The method of claim 1, further comprising generating said output signal from said first and second timing signals, said output signal being generated by generating a falling edge of the output signal in response to the first timing signal and generating a rising edge of the output signal in response to the second timing signal.

6. The method of claim 4, wherein the rising edge of the output signal is generated in response to a rising edge of the delayed clock signal.

7. The method of claim 4, wherein the falling edge of the output signal is generated in response to a rising edge of an inverse of the delayed clock signal.

8. The method of claim 1, wherein said generating of said output signal includes generating said first and second timing signals such that a high time and low time of said output signal is about equal.

9. The method of claim 1, further comprising comparing a signal representative of the output signal with a local clock signal derived from said first

clock signal and generating at least said delayed clock signal in response to a phase difference between the local clock signal and the signal representative of the output signal.

10. The method of claim 9, wherein generating said output signal further comprises phase-locking a rising edge of the first clock signal with a rising edge of the output signal when said phase difference is substantially zero.

11. The method of claim 10, further comprising generating a phase-lock signal in response to said phase-locking of the rising edges of the first clock signal and the output signal.

12. The method of claim 11, further comprising comparing said delayed clock signal with an inverse of said delayed clock signal and adjusting the relative timing of at least said second timing signal according to a difference between a high time of said delayed clock signal and a high time of said inverse of said delayed clock signal.

13. The method of claim 11, further comprising comparing said delayed clock signal with an inverse of said delayed clock signal and adjusting the relative timing of at least said second timing signal according to a difference between a low time of said delayed clock signal and a low time of said inverse of said delayed clock signal.

14. The method of claim 12, wherein said second timing signal is generated from at least said inverse of said delayed clock signal that is adjusted to produce substantially equal time durations between occurrence of said first and second timing signals.

15. The method of claim 12, wherein comparing said delayed clock signal with said inverse of said delayed clock signal is initiated in response to a rising edge of the first clock signal being phase-locked with a rising edge of the output signal.

16. The method of claim 1, wherein said adjusting of the relative timing includes delaying said first timing signal by a fixed number of delays and delaying said second timing signal by a variable number of delays.

17. The method of claim 16, further comprising varying the variable number of delays to produce substantially equal time durations between occurrence of said first and second timing signals.

18. The method of claim 1, wherein said using of said first and second timing signals to generate said output signal includes generating a rising edge of said output signal from said adjusted first timing signal and generating a falling edge of said output signal from said adjusted second timing signal.

19. The method of claim 1, wherein said adjusting of the relative timing to produce substantially equal time durations includes comparing a first high time

of said delayed clock signal with a second high time of an inverse of said delayed clock signal and delaying said second timing signal sufficient to make said first and second high times substantially equal.

20. The method of claim 1, wherein said adjusting of the relative timing to produce substantially equal time durations includes comparing a first low time of said delayed clock signal with a second low time of an inverse of said delayed clock signal and delaying said second timing signal sufficient to make said first and second low times substantially equal.

21. A logic circuit for synchronizing a first clock signal with an output signal, comprising:

means for receiving said first clock signal;

means for delaying said received first clock signal to produce a delayed clock signal;

means for providing a first timing signal associated with one of a rising and falling edge of said delayed clock signal;

means for providing a second timing signal associated with the other of a rising and falling edge of said delayed clock signal;

means for adjusting the relative timing of at least one of said first and second timing signals to produce substantially equal time durations between the occurrence of said first and second timing signals; and

means for using said first and second timing signals to produce said output signal synchronized with said first clock signal, said output signal having a substantially symmetric duty cycle.

22. A data synchronizing circuit comprising:

at least one logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal, and configured to produce at least first and second timing signals each associated with one of a rising and falling edge of said delayed clock signal; and

circuitry coupled to said at least one logic circuit, configured to adjust a relative timing of at least one of said first and second timing signals to produce substantially equal time durations between occurrence of said first and second timing signals, and configured to generate an output signal having a rising edge synchronized with a rising edge of said first clock signal in response to at least said first and second timing signals, said output signal having a substantially symmetric duty cycle.

23. A circuit as in claim 22, wherein said at least one logic circuit includes a phase detector that detects a difference in phase between said local clock signal derived from said first clock signal and a signal representative of said output signal.

24. A circuit as in claim 22, wherein said circuitry includes a comparator that measures a difference between a low time of said delayed clock signal and a low time of an inverse of said delayed clock signal.

25. A circuit as in claim 22, wherein said circuitry includes a comparator that measures a difference between a high time of said delayed clock signal and a high time of an inverse of said delayed clock signal.

26. A circuit as in claim 24, wherein said circuitry includes an arbiter that generates at least two adjustment signals from an error signal output of said comparator, said adjustment signals being used to produce at least one of said first and second timing signals.

27. A circuit as in claim 25, wherein said circuitry includes an arbiter that generates at least two adjustment signals from an error signal output of said comparator, said adjustment signals being used to produce at least one of said first and second timing signals.

28. A circuit as in claim 22, wherein at least one of said circuitry and said at least one logic circuit includes a fixed delay circuit that delays said delayed clock signal by a fixed number of delays and a variable delay circuit that delays said second timing signal by a variable number of delays.

29. A circuit as in claim 28, wherein said variable number of delays is varied to produce substantially equal time durations between occurrence of said first and second timing signals.

30. A data synchronizing circuit, comprising:

a first logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal;

a second logic circuit configured to compare a first delay characteristic associated with said delayed clock signal with a second delay characteristic associated with an inverse of said delayed clock signal;

a third logic circuit configured to generate a first one-shot timing signal at least from said delayed clock signal and a second one-shot timing signal at least from an adjustably delayed signal associated with said inverse of said delayed clock signal;

circuitry coupled to at least said third logic circuit that adjusts said adjustably delayed signal to produce substantially equal time durations between occurrence of said first and second one-shot timing signals;

a fourth logic circuit configured to produce an output signal from at least said first and second one-shot timing signals, said output signal having a substantially symmetric duty cycle.

31. A circuit as in claim 30, further comprising a phase detector that detects a difference in phase between said local clock signal and a signal representative of said output signal.

32. A circuit as in claim 30, wherein said second logic circuit includes a comparator that measures a difference between a low time of said delayed clock signal and a low time of said inverse of said delayed clock signal.

33. A circuit as in claim 30, wherein said second logic circuit includes a comparator that measures a difference between a high time of said delayed clock signal and a high time of said inverse of said delayed clock signal.

34. A circuit as in claim 32, wherein said second logic circuit includes an arbiter that generates at least two adjustment signals from an error signal output of said comparator, said adjustment signals being used to produce said adjustably delayed signal.

35. A circuit as in claim 33, wherein said second logic circuit includes an arbiter that generates at least two adjustment signals from an error signal output of said comparator, said adjustment signals being used to produce said adjustably delayed signal.

36. A circuit as in claim 30, wherein said first logic circuit includes a fixed delay circuit that delays said local clock signal by a fixed number of delays to produce said delayed clock signal and said third logic circuit includes a variable

delay circuit that delays said inverse of said delayed clock signal by a variable number of delays.

37. A circuit as in claim 36, wherein said variable number of delays is varied by said circuitry to produce substantially equal time durations between occurrence of said first and second one-shot timing signals.

38. A processor system comprising:

a processor;

a memory device connected to the processor, wherein at least said memory device includes a synchronizing circuit comprising:

at least one logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal, and configured to produce at least first and second timing signals each associated with one of a rising and falling edge of said delayed clock signal; and

circuitry coupled to said at least one logic circuit, configured to adjust a relative timing of at least one of said first and second timing signals to produce substantially equal time durations between occurrence of said first and second timing signals, and configured to generate an output signal having a rising edge synchronized with a rising edge of said first clock signal in response to at least said first and second timing signals, said output signal having a substantially symmetric duty cycle.

39. A processor system, comprising:

a processor;

a memory device connected to the processor, wherein at least said memory device includes a synchronizing circuit comprising:

a first logic circuit configured to produce a delayed clock signal from a local clock signal derived from a first clock signal;

a second logic circuit configured to compare a first delay characteristic associated with said delayed clock signal with a second delay characteristic associated with an inverse of said delayed clock signal;

a third logic circuit configured to generate a first one-shot timing signal at least from said delayed clock signal and a second one-shot timing signal at least from an adjustably delayed signal associated with said inverse of said delayed clock signal;

circuitry coupled to at least said third logic circuit that adjusts said adjustably delayed signal to produce substantially equal time durations between occurrence of said first and second one-shot timing signals;

a fourth logic circuit configured to produce an output signal from at least said first and second one-shot timing signals, said output signal having a substantially symmetric duty cycle.

40. The method of claim 3 wherein said timing signal is a strobe signal.

41. A circuit of claim 21 wherein said output signal is a data output signal.

42. A circuit of claim 21 wherein said output signal is a data timing output signal.

43. A circuit of claim 42 wherein said data timing output signal is a strobe signal.

44. A circuit of claim 22 or 30 wherein said output signal is a data output signal.

45. A circuit of claim 22 or 30 wherein said output signal is a data timing output signal.

46. A circuit of claim 45 wherein said data timing output signal is a strobe signal.

47. A system of claim 38 or 39 wherein said output signal is a data output signal.

48. A system of claim 38 or 39 wherein said output signal is a data timing output signal.

49. A system of claim 48 wherein said data timing output signal is a strobe signal.